

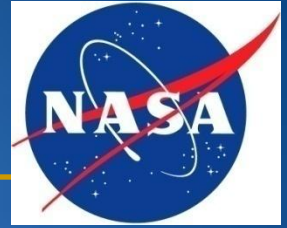
**2010 INTERNATIONAL WORKSHOP ON ENVIRONMENT AND  
ENERGY**

# **LEAD-FREE TECHNOLOGY EXPERIMENT IN A SPACE ENVIRONMENT (LTESE)**

**Jim Blanche/Jacobs ESTS Group**

**Marshall Space Flight Center  
Huntsville, Alabama**

# Lead-free Technology Experiment in Space Environment (LTESE)



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**Implementing Organization POC: MSFC/ES43/Melanie Bodiford**  
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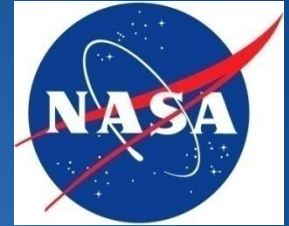
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**Power System Engineer: MSFC/ES41/David O'Dell**  
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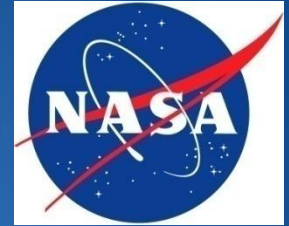
# Lead-free Technology Experiment in a Space Environment (LTESE)



## JUSTIFICATION

**LTESE is a response to the Joint Council on Aging Aircraft (JCAA)/ Joint Group on Pollution Prevention (JG-PP) Lead-Free Solder Project, Joint Test Report, July 27, 2007 recommendations that next steps for aerospace and defense Pb-free applications include experiments to determine the effect of higher reflow temperatures on printed wiring boards and functional integrated circuits, and to gather data in operational environments. LTESE is gathering data in operational environments.**

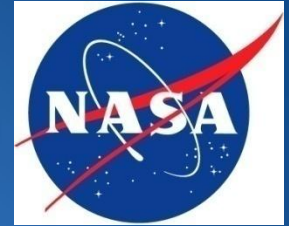
# Lead-free Technology Experiment in a Space Environment (LTESE)



## JUSTIFICATION (cont'd)

**While there is no doubt that Pb-free electronic parts have flown in space before, they have never flown under totally known recorded conditions and been available for complete post flight failure analysis. That is the case with this experiment which is part of the seventh Materials on International Space Station Experiment (MISSE 7).**

# What is MISSE (Materials on International Space Station Experiment)



(1) MATERIALS IN HOLDER



(2) HOLDERS IN TRAY



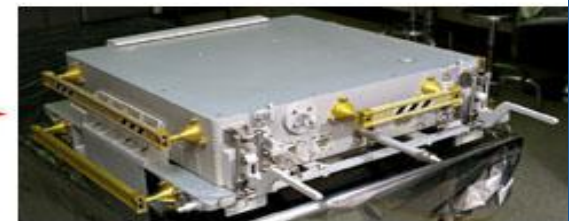
PEC CARRIER



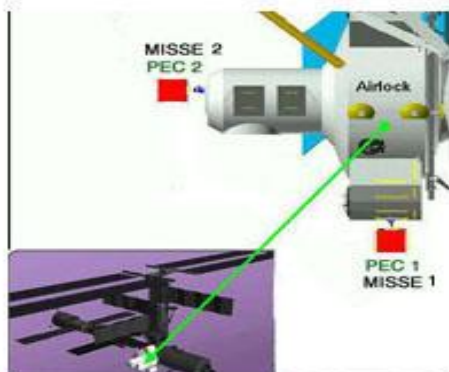
EMPTY PEC



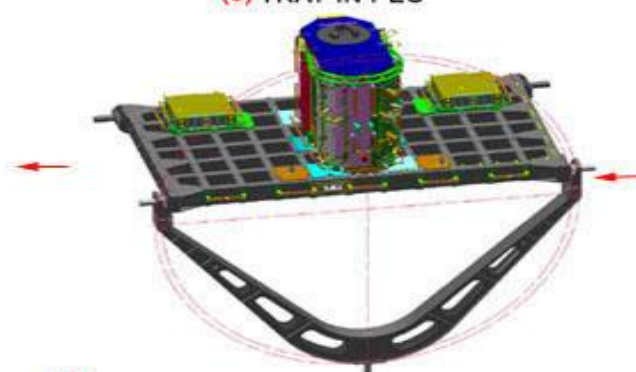
(3) TRAY IN PEC



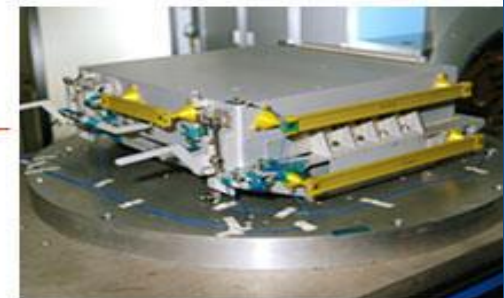
(4) PEC IN CARRIER



(7) PEC ATTACHED TO SPACE STATION



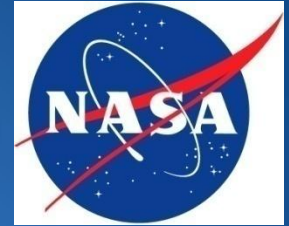
(6) PEC INSTALLED ON SHUTTLE BAY TRUSS



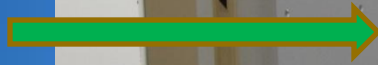
(5) VIBRATION TEST

# MISSE 7

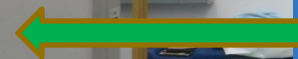
## Passive Experiment Containers A & B



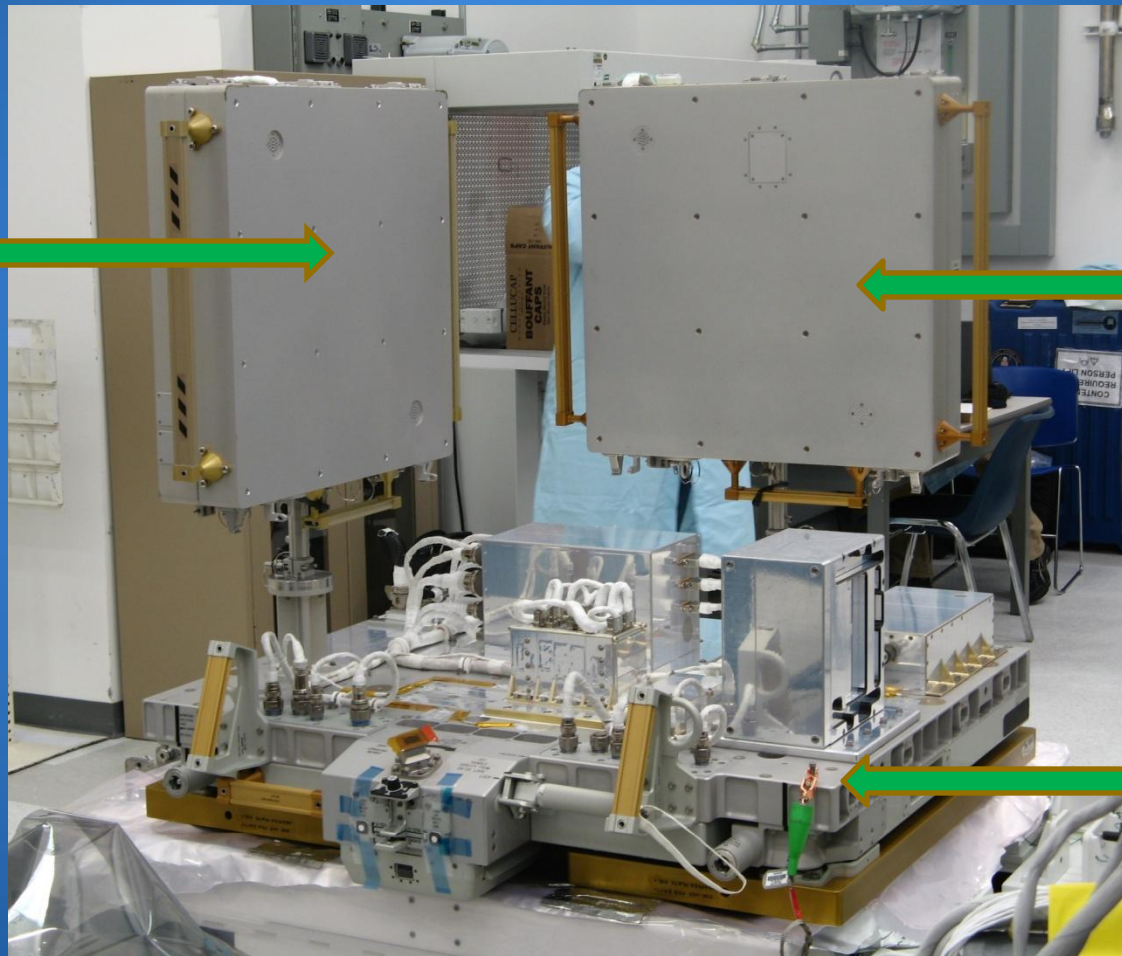
PEC B



PEC A

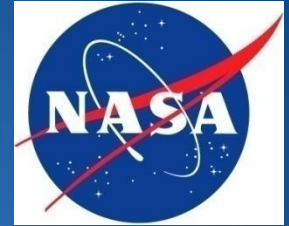


EXPRESS  
LOGISTICS  
CARRIER



# MISSE 7

## Passive Experiment Containers A & B



PEC B



PEC A

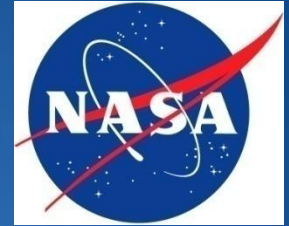
# Lead-free Technology Experiment in a Space Environment (LTESE)



## LTESE BENEFITS

The Constellation Program Workmanship Requirements document (CxP 70165) prohibits use of lead-free technology. Engineering technical authority requires space environment data in order to assess risk and make recommendations to Material Review Boards and Project Offices when lead-free technology is incorporated into flight hardware inadvertently or through the use of commercial off-the-shelf (COTS) hardware.

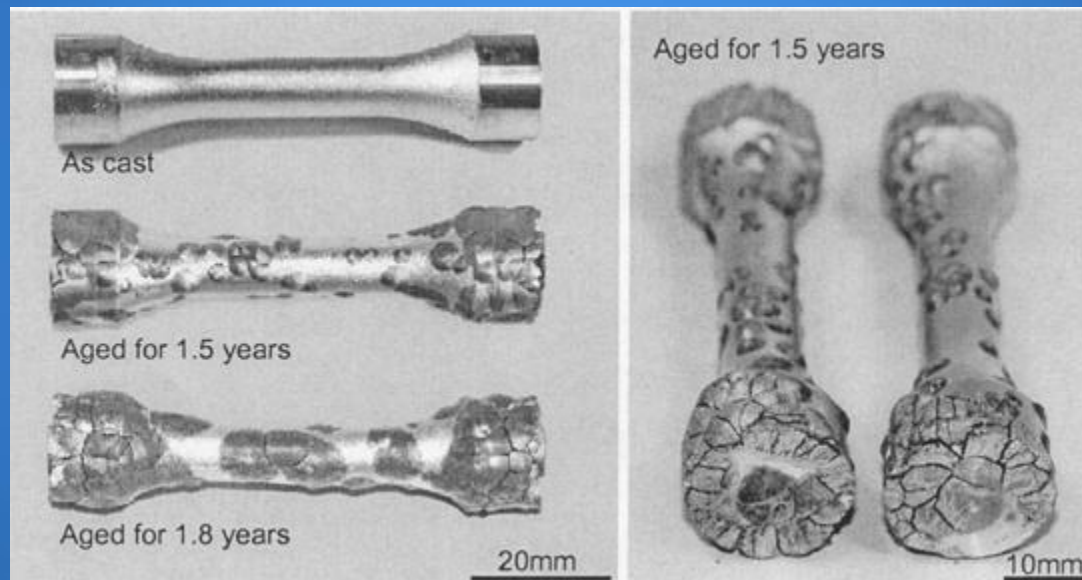
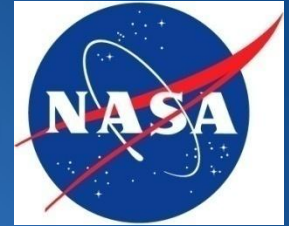
# Lead-free Technology Experiment in a Space Environment (LTESE)



## EXPECTED RESULTS

- Intermetallic Compound (IMC) formation and growth under near zero gravity and various temperatures.
- Pb-free solder joint life under temperature extremes.
- Aging effects on Pb-free solder joints in space environments.
- Results of launch and reentry dynamics.
- Tin whisker growth under known space conditions.
- Possibly the formation of tin pest which can initiate at 13°C.
- All data to be compared to a ground unit operating for the same time in a lab environment.

# Lead-free Technology Experiment in a Space Environment (LTESE)



## Tin Pest

# Lead-free Technology Experiment in a Space Environment (LTESE)

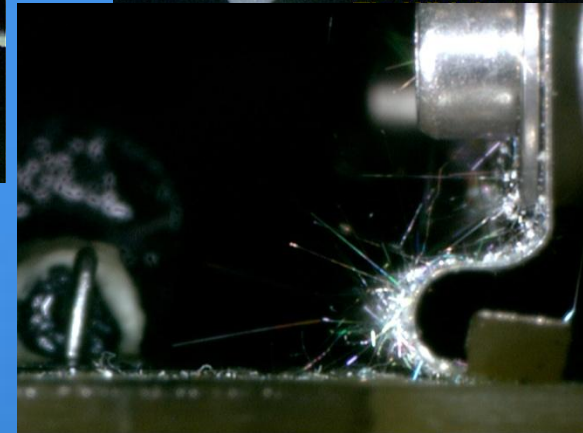
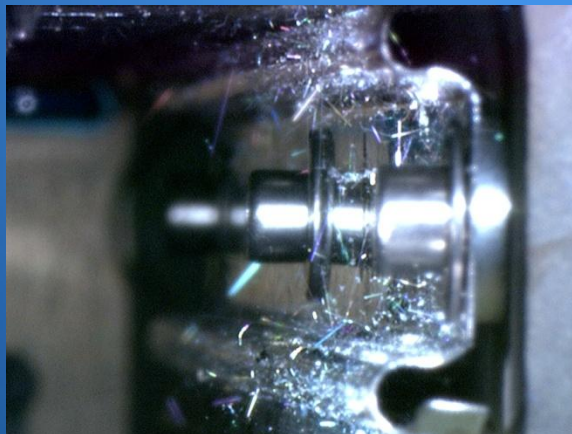
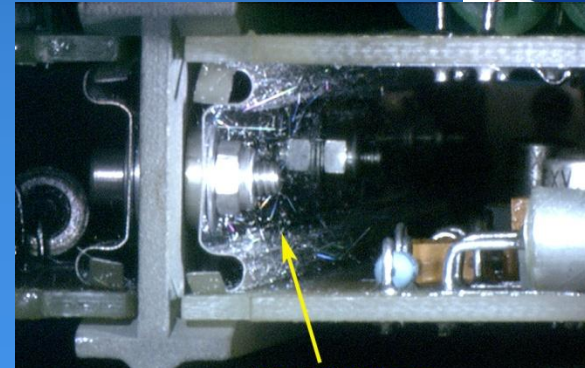
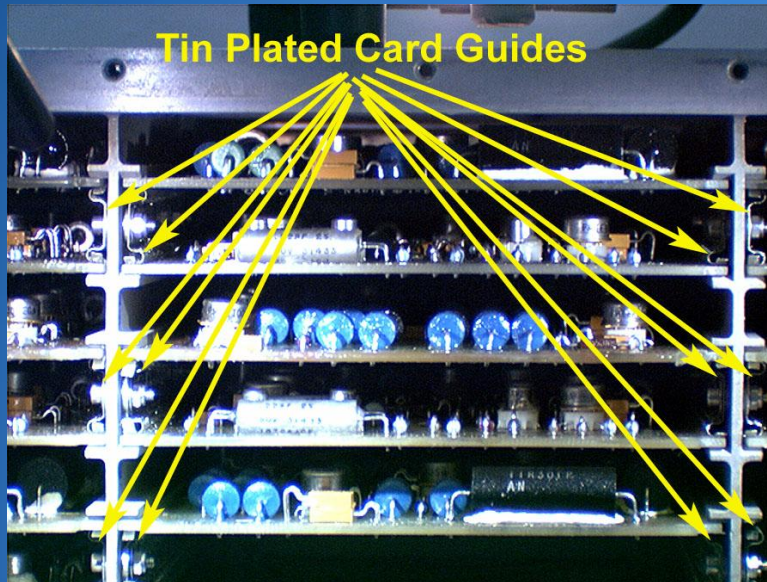
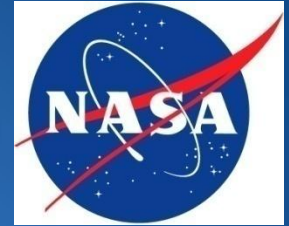


Figure 1. View of tin whiskers on card guide surface of ATV Control (S/N 0034). Many of these whiskers exceed 5 mm in length.

## Tin Whiskers

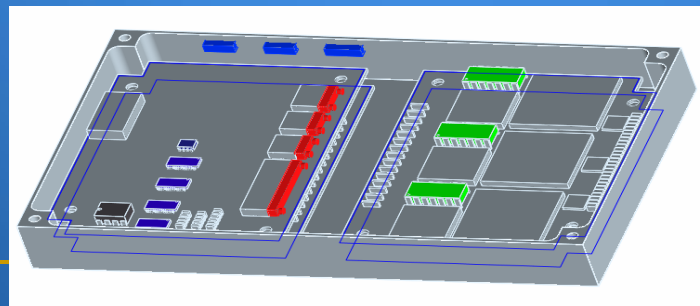
# Lead-free Technology Experiment in a Space Environment (LTESE)



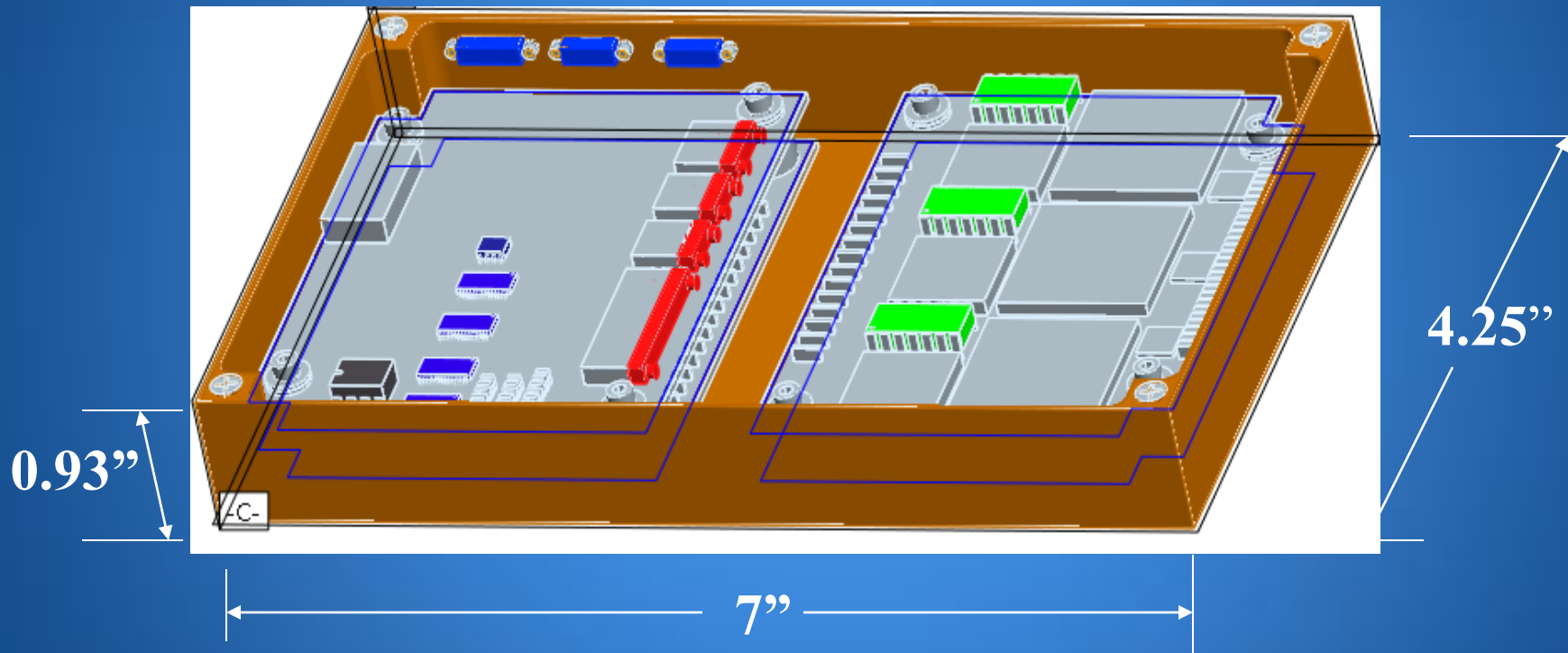
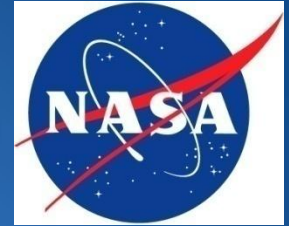
## DESCRIPTION

The Lead-Free Technology Experiment in Space Environment (LTESE) experiment is a small active package containing three test boards and one data acquisition system:

- One immersion silver finished board with Pb-free parts using Pb-free solder (COTS simulation)
- One SnPb finished board with Pb-free parts using SnPb solder (Inadvertent incorporation)
- One SnPb finished board with SnPb parts using SnPb solder (Control board)
- One data system board
- Desired environment is exposure to space environment for ~1 year



# LTESE Mechanical Specifications

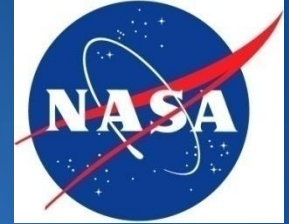


**Weight : 417 gms/0.92 lbs**

**Coating: CHEMICAL CONVERSION COAT PER MIL-DTL-5541 TYPE II, CLASS 3**

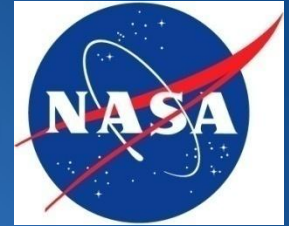
**Note: Cover and cabling not shown for clarity**

# Test Board Fabrication

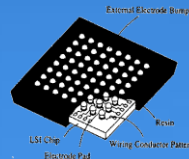


- **Pb-free test parts are:**
  - ❑ 256 I/O PBGAs with SAC405 balls (Large area array)
  - ❑ 100 I/O CSPs with SAC405 balls (Small area array)
  - ❑ 0805 zero ohm resistors with a SAC305 finish (Chip part)
  - ❑ 100 lead QFPs with 100% Sn finish (Leaded SMT part)
  - ❑ 14 lead PDIPs with 100% Sn finish (Through-hole part)
- **Sn63Pb37 with an Sn63Pb37 profile has been used to solder the Pb-free parts into the SnPb boards**
- **Sn3.0Ag0.5Cu (SAC305) solder has been used for the Pb-free boards**

# Test Board Fabrication



**BALL GRID ARRAY**



**CHIP SCALE PACKAGE**



**DUAL IN-LINE PACKAGE**



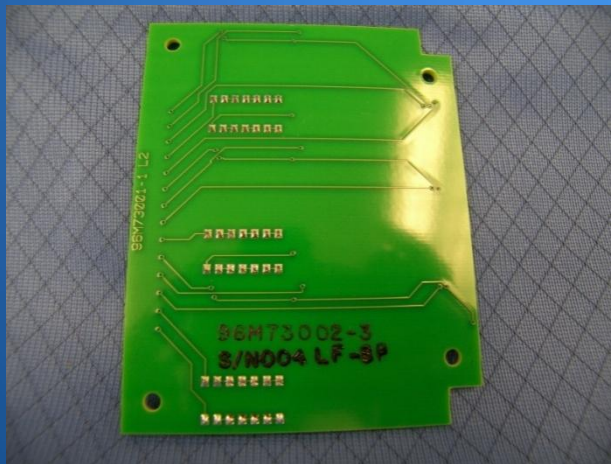
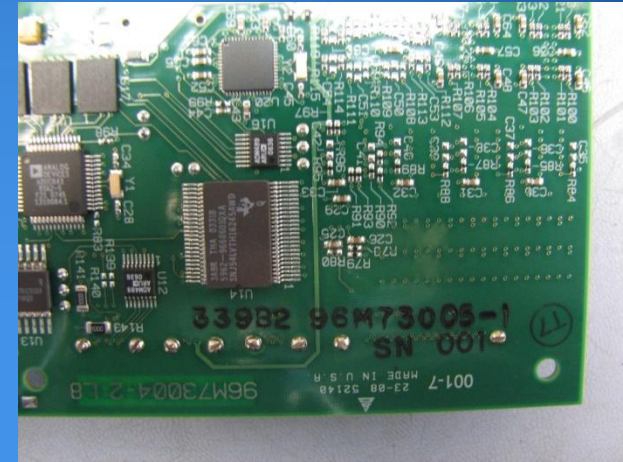
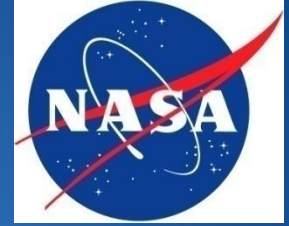
**QUAD FLATPACK**



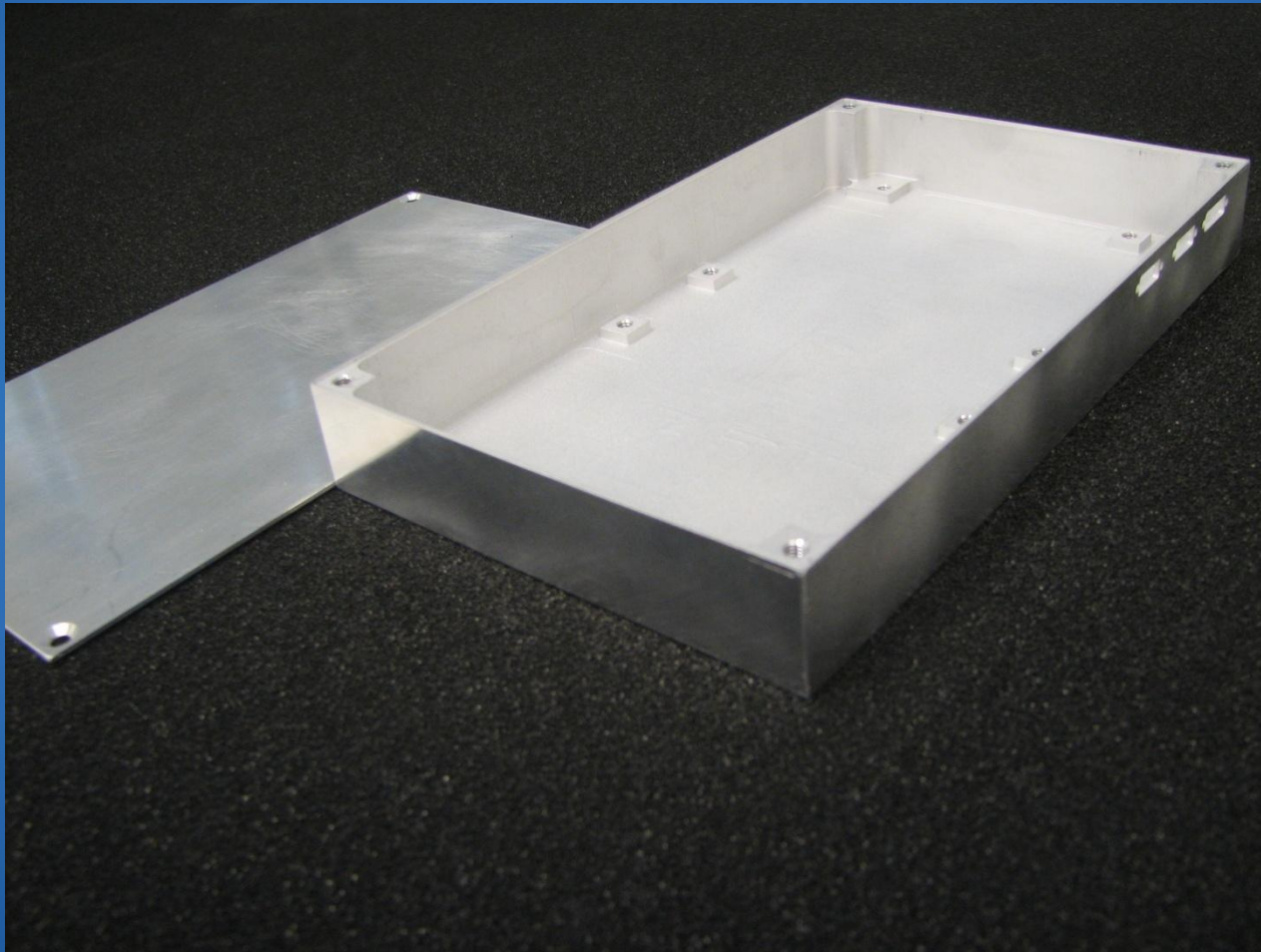
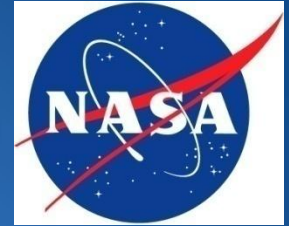
**0805 CHIP RESISTOR- .080"x.050"**

## Lead-free Test Parts

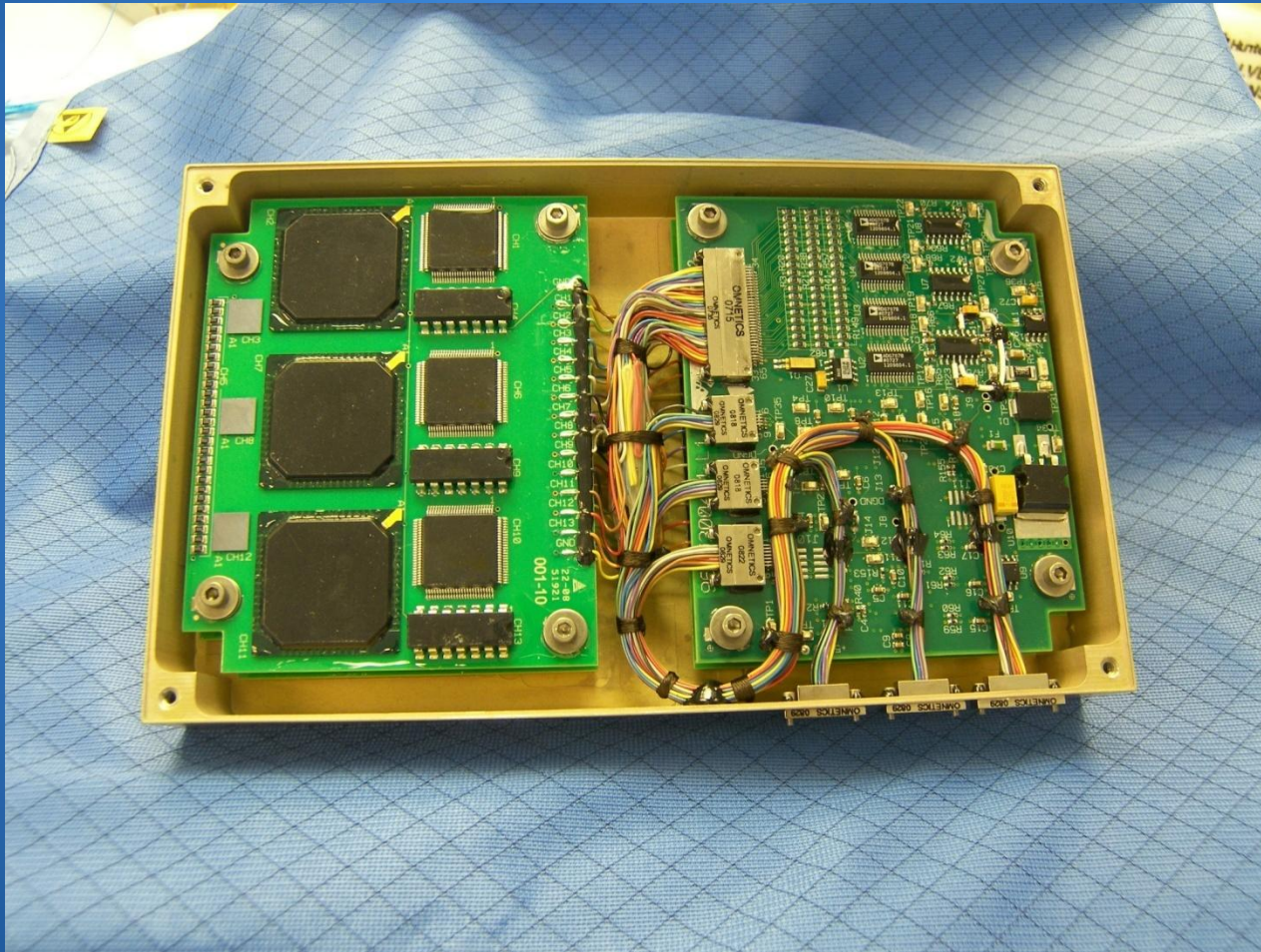
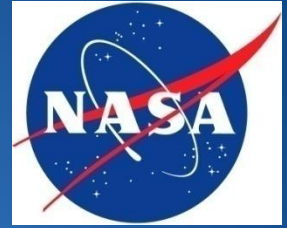
# LTESE Test and Data Boards



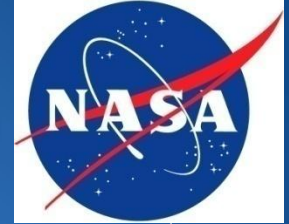
# LTESE Housing



# LTESE Package

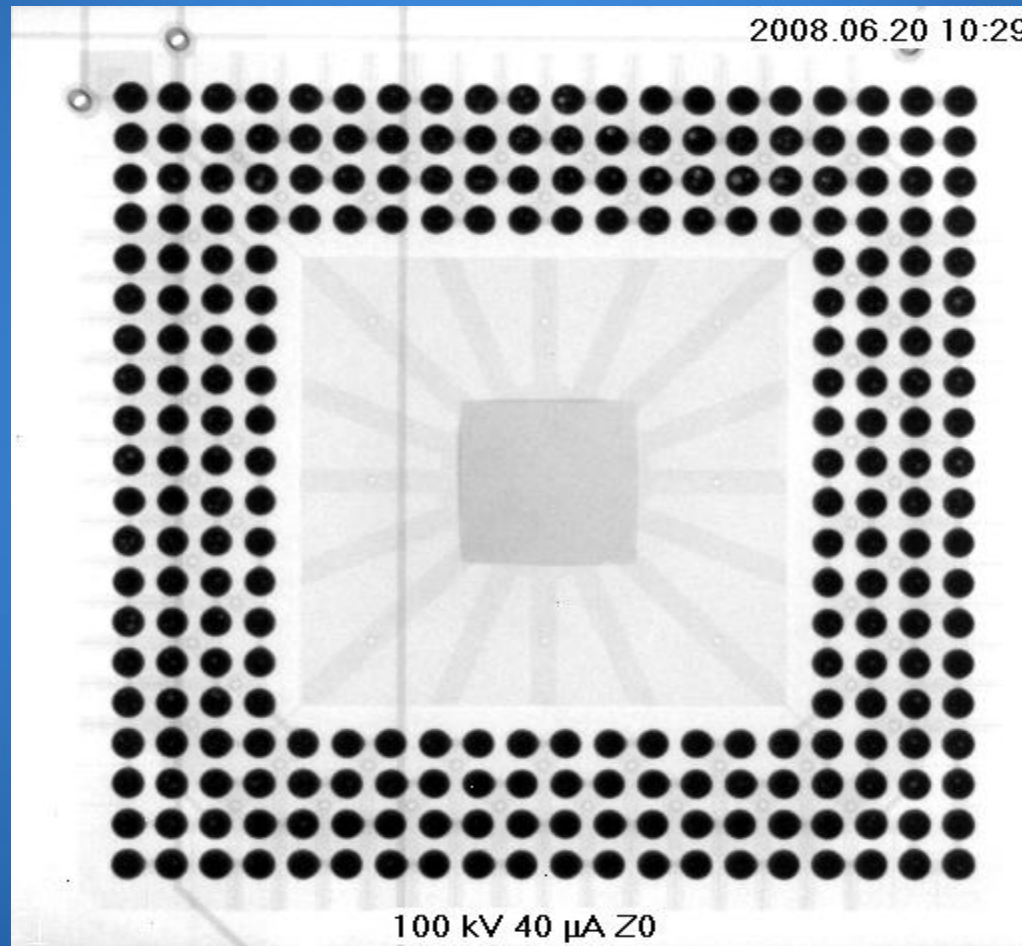
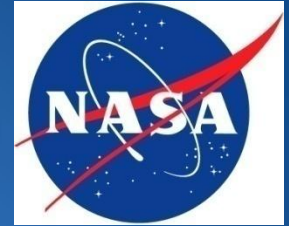


# Test Board Fabrication

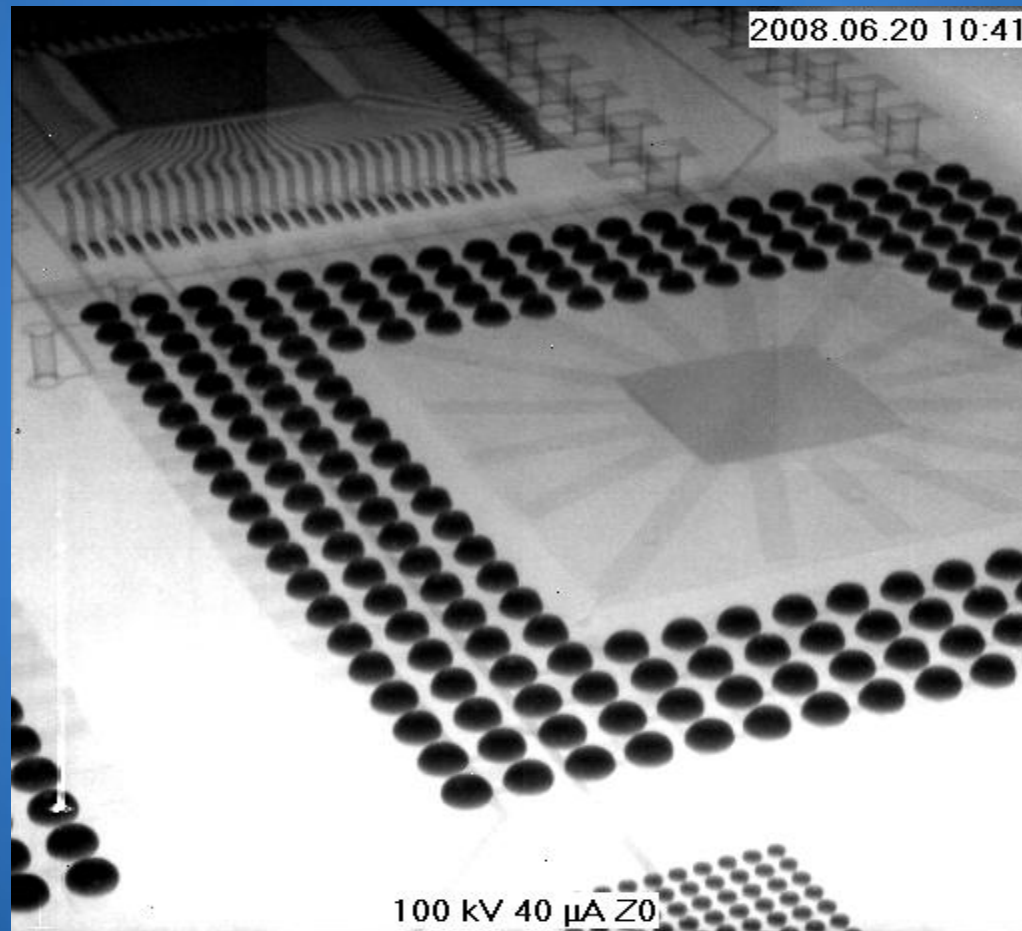
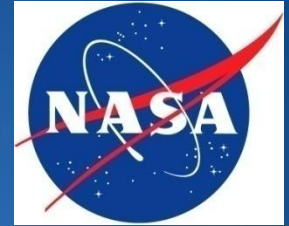


- All test parts are daisy chained dummy parts (1464 solder joints per test board)
- Each part forms one test circuit except all 27 chip resistors form a single circuit
- All test boards vapor phase soldered
- Sn/Pb used 217°C vapor , Pb-free used 240°C vapor
- All board assemblies cleaned in vapor degreaser and conformal coated with Solithane 113-300

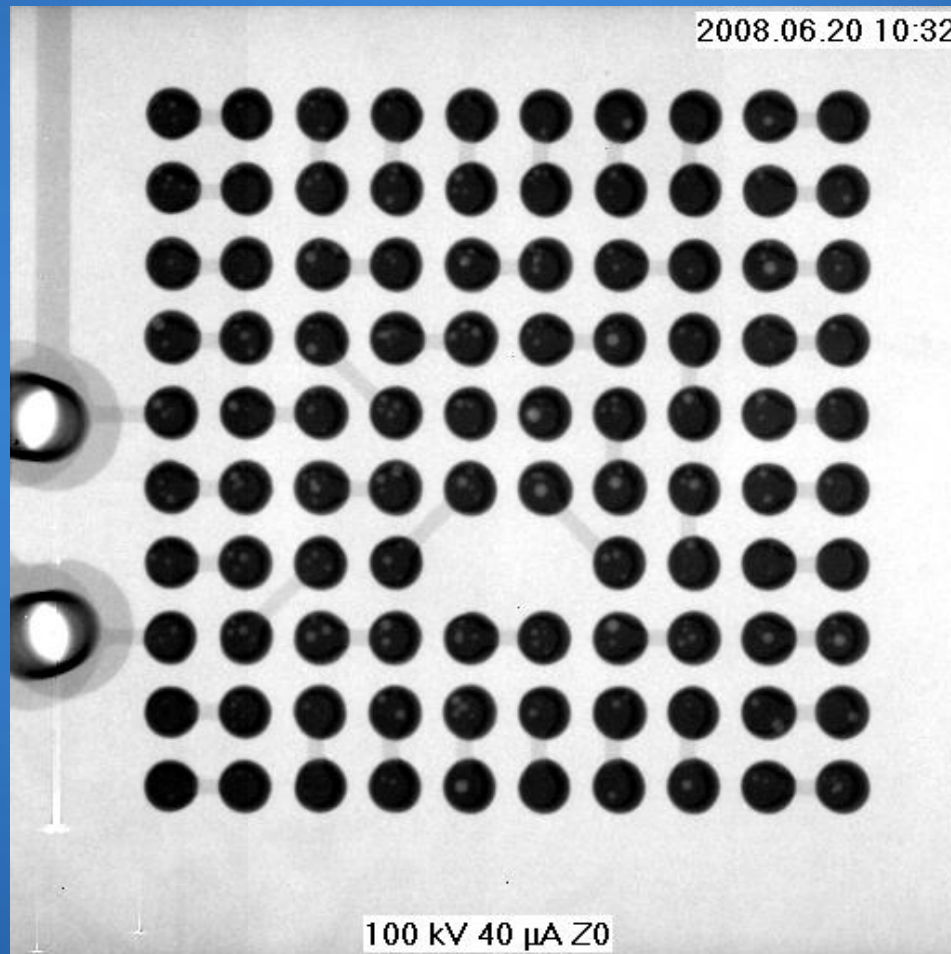
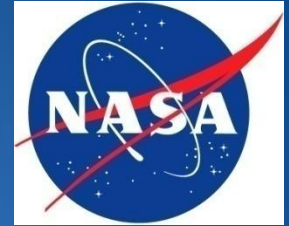
# S/N 007 Pb-free/Pb-free BGA X-Ray



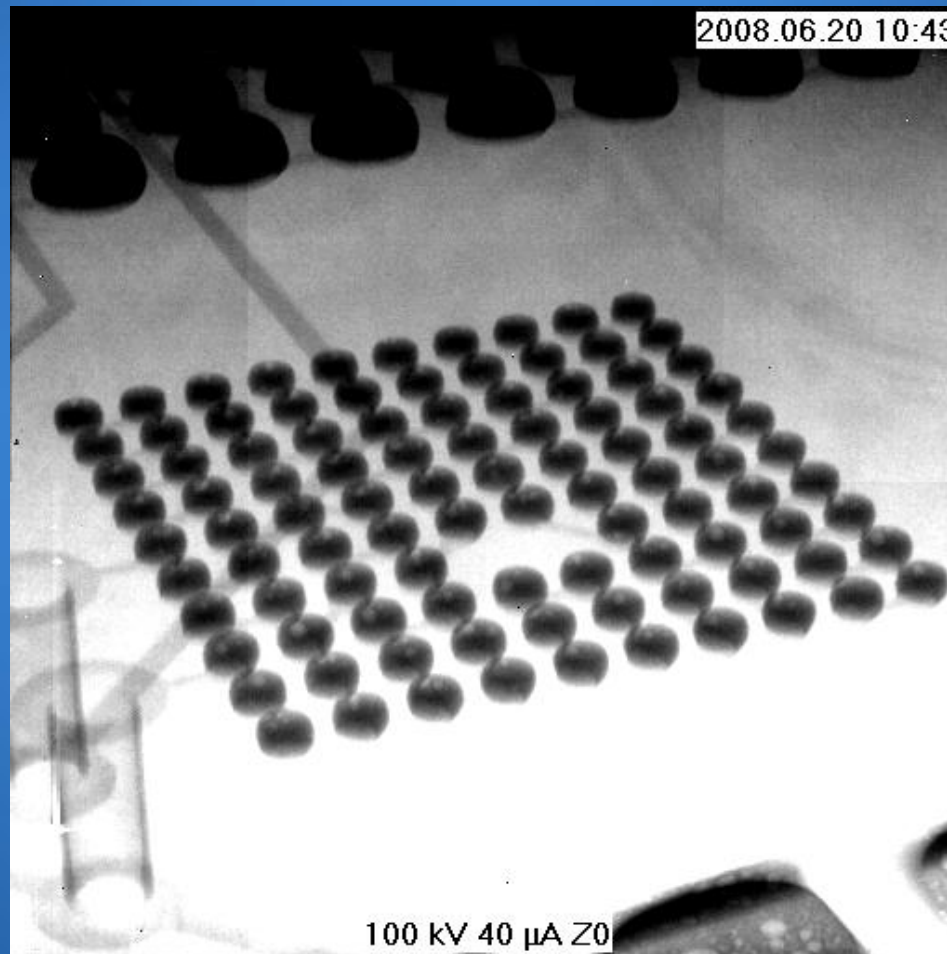
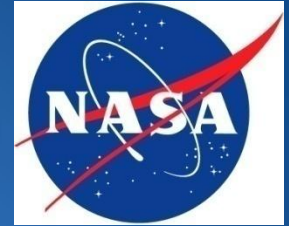
# S/N 007 Pb-free/Pb-free BGA X-Ray, Oblique



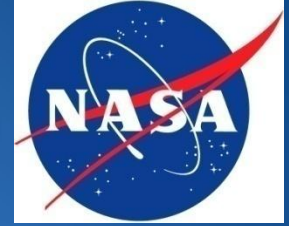
# S/N 007 Pb-free/Pb-free CSP X-Ray



# S/N 007 Pb-free/Pb-free CSP X-Ray, Oblique



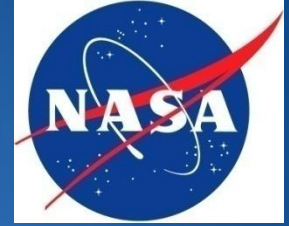
# LTESE Electrical Characteristics



## Power:

- Voltage and current from MISSE: +15V @ ~800mA peak
- Converted to +5.1V and +3.3V on LTESE data system board
- Max Pwr: ~800mA
- Average Pwr: ~450mA
- Power Consumption: 12.2 W Maximum, 6.85 W Average

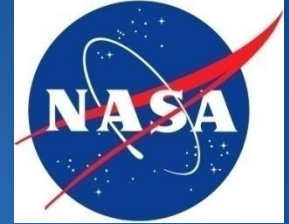
# LTSESE Electrical Characteristics



## Power:

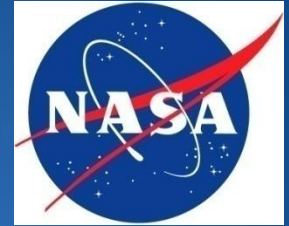
- **Duty Cycle:** MISSE-7B has proposed a ping every 5 minutes.
  - ❑ The data system will be on for approximately 10 seconds to record, downlink, and store the data.
  - ❑ Digital section of the board will be put to sleep between pings from MISSE, but 200 mA current source feeding analog channels will always be powered

# Concept of Operations



- **Data Card is designed to record the resistance of each circuit and temperature in the box every 6 minutes for the time on the outside of the Station.**
- **Temperature sensor is located on the data board**
- **Parts are daisy chained and resistance of each part is being recorded individually.**
- **A duplicate package on the ground is recording the same data for comparison.**

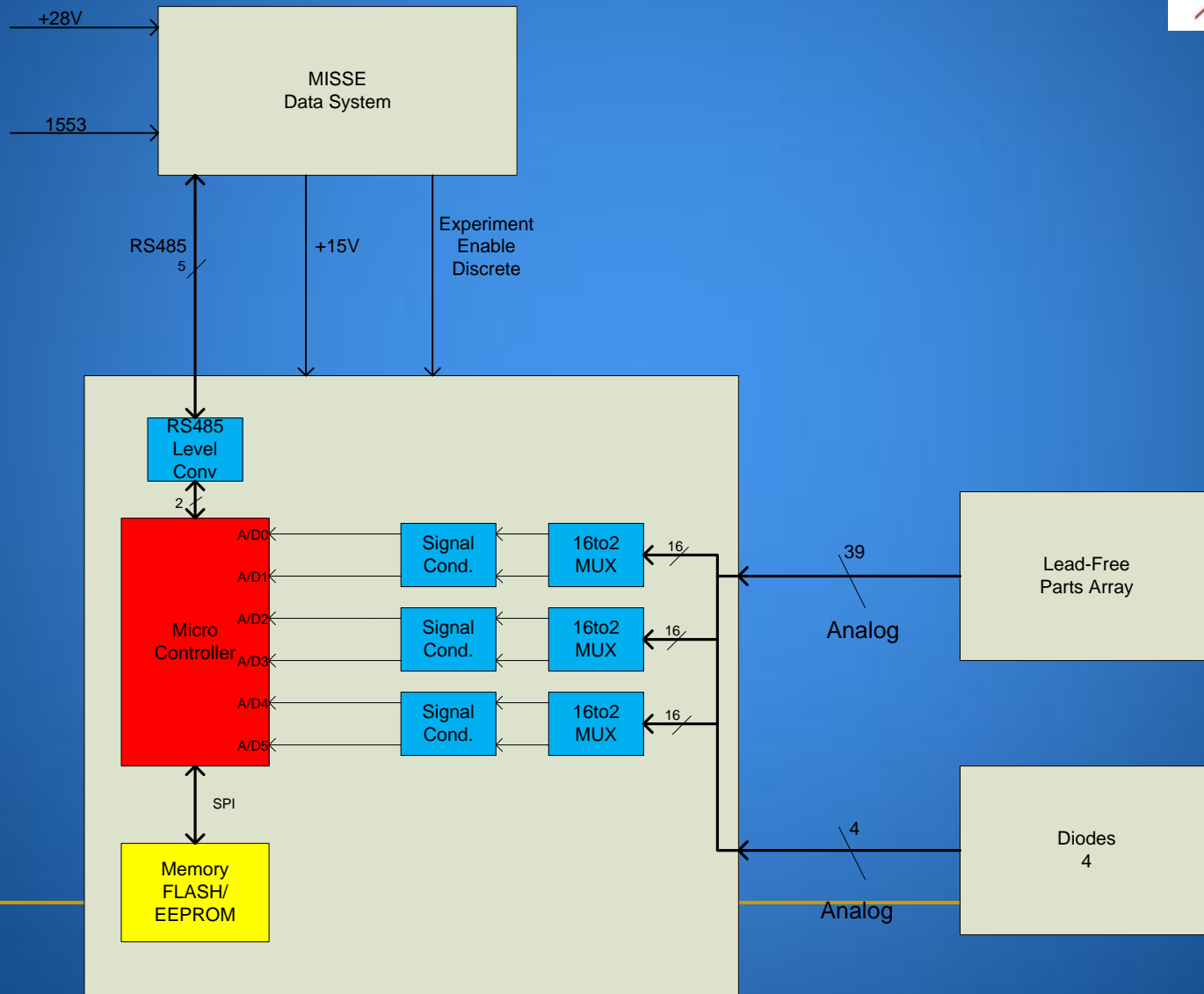
# Concept of Operations



## Data System Operation:

- When MISSE sends signal asking for sample, data system will take a measurement from our 39 test channels and the external diodes.
  - If data system loses communication with MISSE, will use real-time clock for timing and will store data to internal FLASH memory only.
- Timestamp and health/status will be appended to the experiment data.
- Data will then be transmitted to the ground and will also be stored to triple redundant FLASH memory.

# LTESE Data System Block Diagram

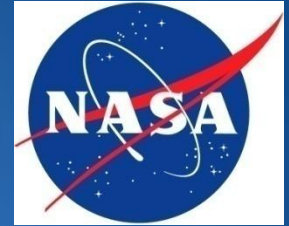


# LTESE Risks



- Minimal rad tolerance (RS485 xmit logic is the only rad tolerant part of design)
- Plastic parts, subject to temperature extremes
- Lack of end-to-end test from LTESE through MISSE-7B, ELC, ISS and ground data systems

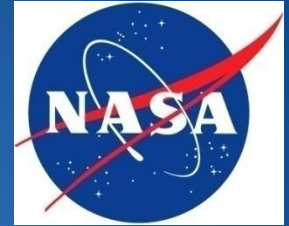
# Lead-free Technology Experiment in a Space Environment (LTESE)



## Status

- All hardware was designed, manufactured and assembled at MSFC.
- CDR conducted 6/17/08. No issues.
- Integration into MISSE 7 successfully completed.

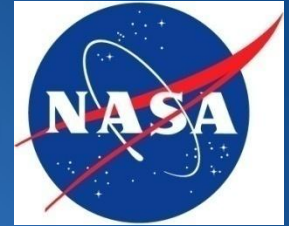
## Lead-free Technology Experiment in a Space Environment (LTESE)



### Status (cont'd)

- LTESE was launched on STS129 11/16/2009
- Spacewalker Randy Bresnik completed installation of the MISSE 7 experiment on Express Logistics Carrier 2 on 11/22/09
- LTESE first powered up on the Station 11/23/09
- LTESE is scheduled for return on STS134 no earlier than February 2011

# Lead-free Technology Experiment in a Space Environment (LTESE)



## Status (cont'd)

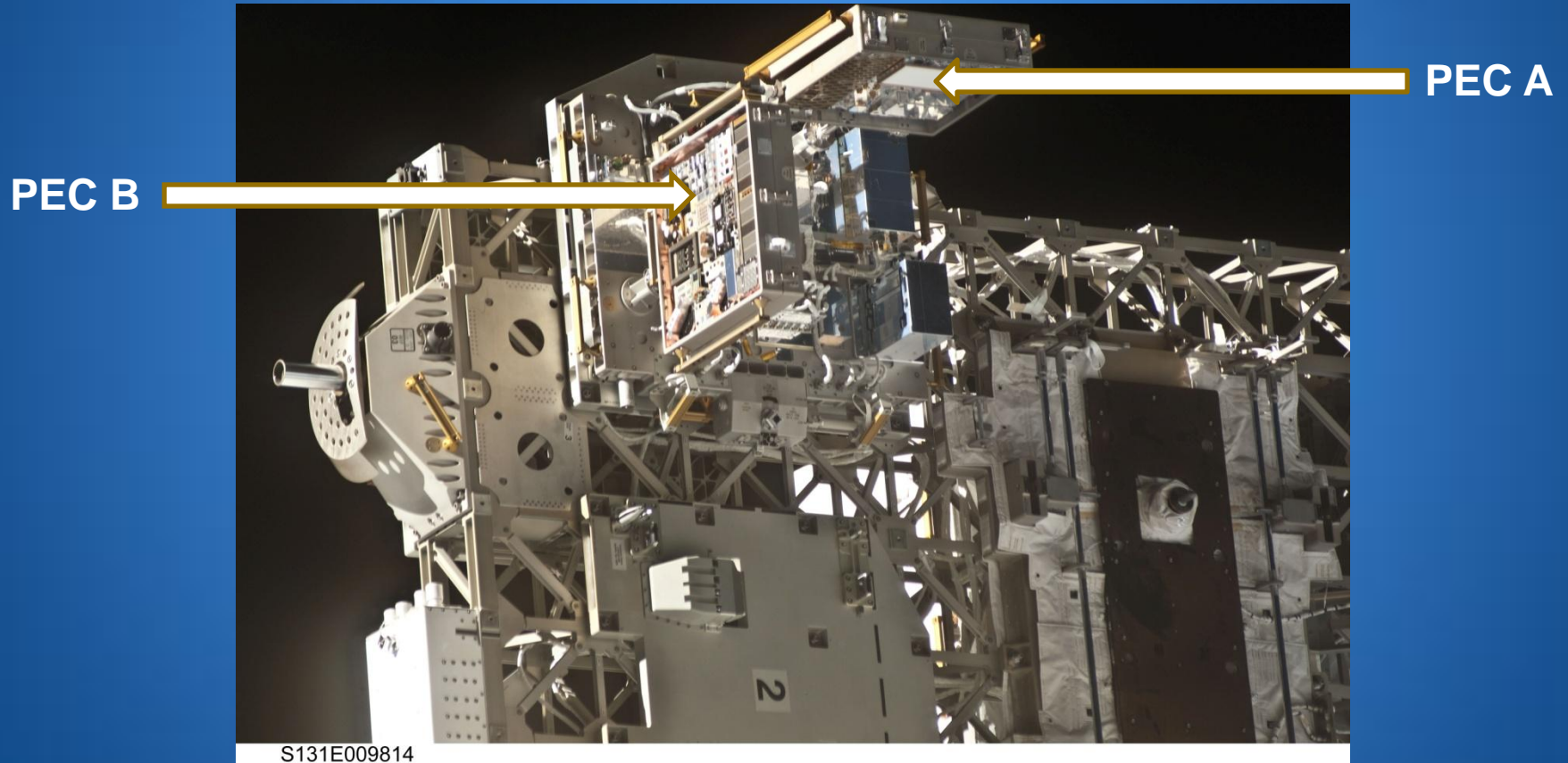
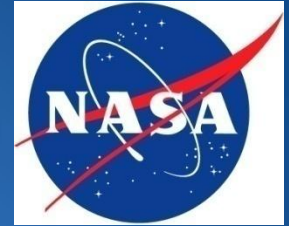
- Due to some controller issues on the spacecraft side data from LTESE is not available for downlinking but is being recorded on the internal triple redundant FLASH memory
- MISSE7-B is a Naval Research Lab package and they have set temperature limits on it of -40°C to +50°C
- MISSE7-B will be powered down approximately 70 days during its year on Station
- The ground unit was powered up on 12/4/09 and will run till the flight unit is removed from the Station for return

## Lead-free Technology Experiment in a Space Environment (LTESE)

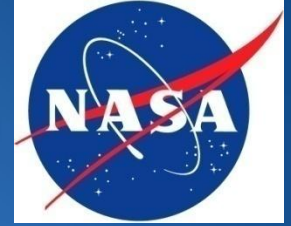
### Status (cont'd)

- There have been no primary controller error messages from the Space Station so it is assumed that the controller is working and that the flash memories are recording data
- The ground unit was checked 10/4/10 and the error fields were clear and the voltages for the samples looked good so there were no solder joint failures after 296 days of operation

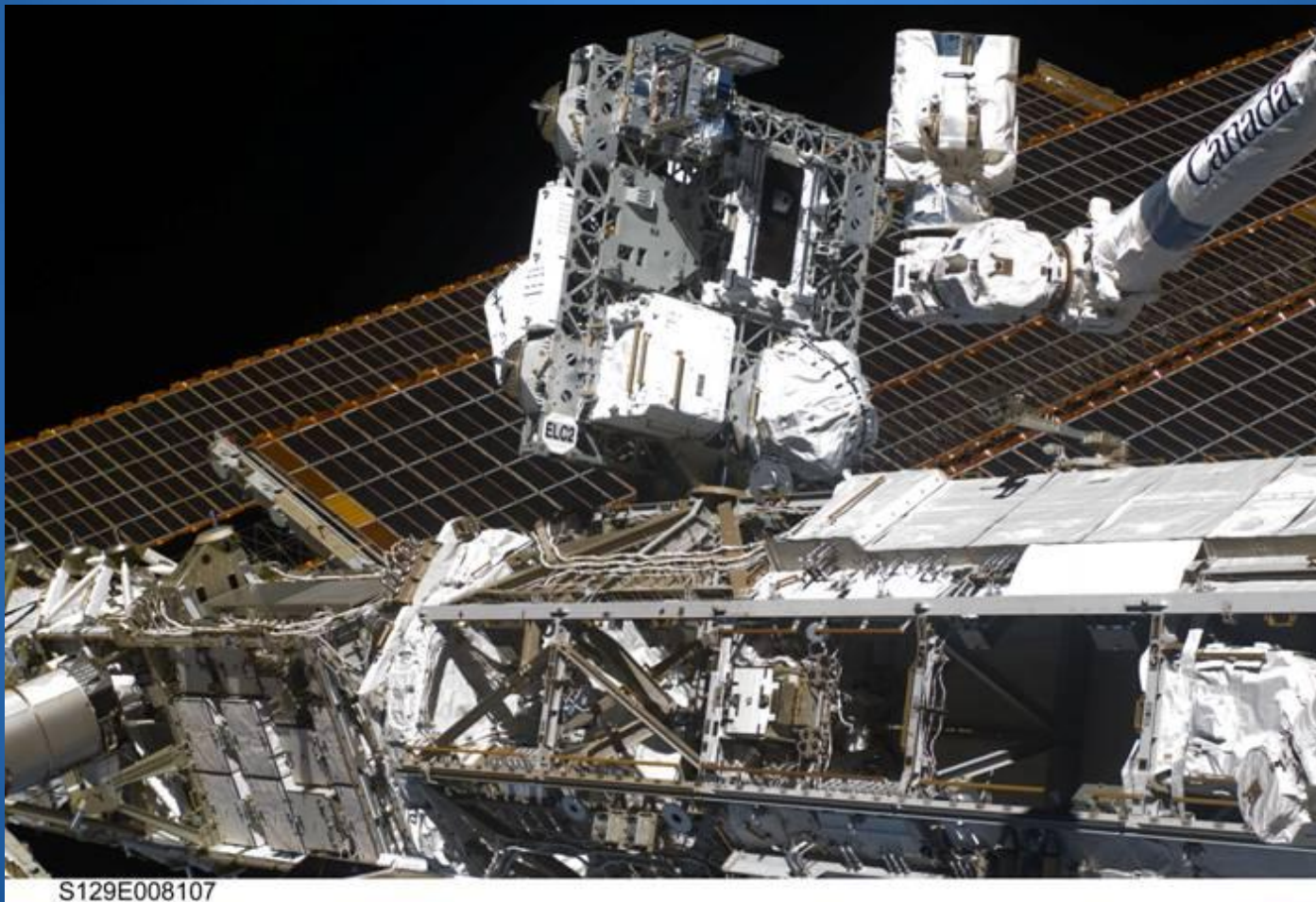
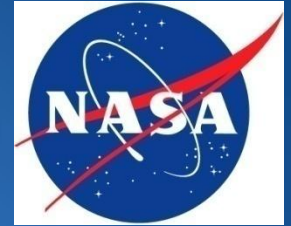
# MISSE 7 on ISS



# MISSE 7 on ISS

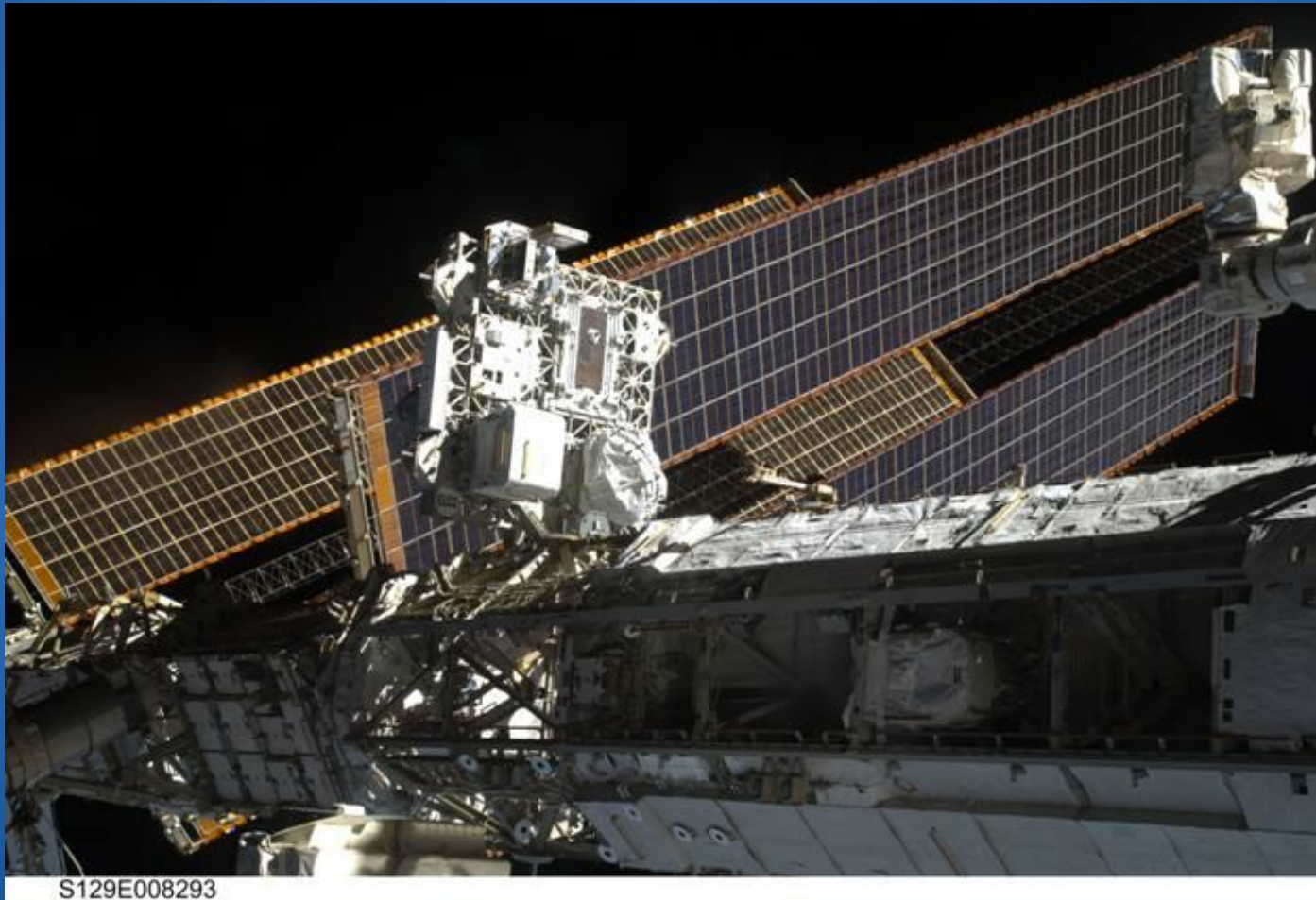
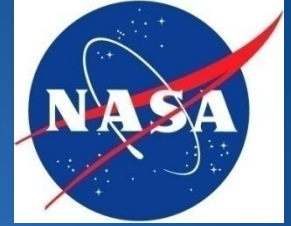


# MISSE 7 on ISS

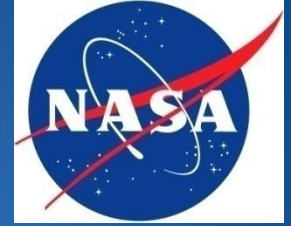


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# MISSE 7 on ISS



# MISSE 7 on ISS



# Questions???

